IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 5, 12, 24 and 30 and AMEND claims 1, 11, 20, 29 and 36 in accordance with the following:

1. (CURRENTLY AMENDED) A processing apparatus comprising:

an internal circuit comprising:

a CPU executing programs, said CPU is supplied with a first clock and executes the programs synchronously with the supplied first clock, and,

at least one internal device having a predetermined function, and

a bus line extending internally of the internal circuit and connecting said CPU to said internal device, the bus line comprising an externally extending portion extending externally of the internal circuit and an address bus and a data bus transferring an address and data, respectively, wherein said internal circuit includes at least one internal memory as an internal device, the internal memory storing a program for determining ciphering patterns; and

an external circuit provided externally of the internal circuit and connected with the externally extending portion of said bus line and including at least one external device having a predetermined function, wherein said external circuit includes at least one external memory as an external device, wherein

said internal circuit further comprises a ciphering section interposed at an entrance to an external side of said internal circuit, and ciphering the address and the data on the bus line by the ciphering patterns according to a plurality of regions divided from an address space allotted to entirety of said at least one external device, to thereby prevent illicit access to the internal memory via the external memory, said ciphering section is supplied with a second clock and performs ciphering synchronously with the supplied second clock and a clock supply section for supplying a first clock at a higher speed than a speed of the first clock supplied to said CPU, to said ciphering section.

2. (ORIGINAL) A processing apparatus according to claim 1, wherein

the ciphering patterns adopted by said ciphering section include one ciphering pattern in which neither the address nor data is ciphered.

3. (ORIGINAL) An processing apparatus according to claim 1, wherein

said external circuit includes a plurality of external devices; and

said ciphering section performs ciphering using ciphering patterns according to said plurality of external devices, respectively.

4. (ORIGINAL) A processing apparatus according to claim 1, wherein

said ciphering section outputs a dummy address and dummy data to the externally extending portion of said bus line at timing at which said external circuit is not accessed.

5. (CANCELLED)

6. (ORIGINAL) A processing apparatus according to claim 1, comprising:

ciphering pattern determination means for recognizing a constitution of said external circuit and determining a ciphering pattern of said ciphering section according to the constitution of said external circuit.

7. (ORIGINAL) A processing apparatus according to claim 1, wherein

said ciphering section ciphers the address and the data on said bus line by ciphering patterns according to the plurality of regions divided from the address space allotted to the entirety of said no less than one external device and according to application programs executed by said CPU.

8. (ORIGINAL) A processing apparatus according to claim 1, comprising:

a deciphering section connected to the externally extending portion of said bus line, and returning the ciphered address and the data on the bus line to an address and data which are not ciphered.

9. (ORIGINAL) A processing apparatus according to claim 1, comprising:

ciphering pattern change means for changing a ciphering pattern whenever a predetermined initialization operation is carried out for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device.

10. (ORIGINAL) A processing apparatus according to claim 1, wherein

said ciphering section adopts a ciphering pattern in which ciphered data is changed according to the address, for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device, to thereby cipher the data.

11. (CURRENTLY AMENDED) A processing apparatus comprising:

an internal circuit comprising:

a CPU executing programs,

at least one internal device having a predetermined function, and

a bus line extending internally of the internal circuit and connecting said CPU to said internal device, the bus line comprising an externally extending portion extending externally of the internal circuit and an address bus and a data bus transferring an address and data, respectively, wherein said internal circuit includes at least one internal memory as an internal device~~, the internal memory storing a program for determining ciphering patterns~~; and

an external circuit provided externally of the internal circuit and connected with the externally extending portion of said bus line, and storing information, wherein said external circuit includes at least one external memory as an external device, wherein

said internal circuit has information rewrite means for ciphering and rewriting at least part of the information stored in said external memory in a predetermined initialization operation, to thereby prevent illicit access to the internal memory via the external memory and said predetermined initialization operation is an initialization operation when the apparatus is first powered on.

12. (CANCELLED)

13. (ORIGINAL) A processing apparatus according to claim 11, wherein

said information rewrite means generates a random number, and performs ciphering by adopting a ciphering pattern using the generated random number.

14. (PREVIOUSLY PRESENTED) A processing apparatus according to claim 11, wherein

the at least part of the information stored in said external memory has been already ciphered before said predetermined initialization operation is carried out; and

said information rewrite means temporarily returns the at least part of the information to information which is not ciphered, and rewrites the information by ciphering again the information by adopting a different ciphering pattern.

15. (ORIGINAL) A processing apparatus according to claim 14, wherein

deciphering information for returning said at least part of information to information before being ciphered is stored in said memory; and

said information rewrite means temporarily returns the at least part of information to the information before being ciphered using the deciphering information.

16. (ORIGINAL) A processing apparatus according to claim 14, wherein

said at least part of information is ciphered by a public key, and a secret key is embedded in this processing apparatus; and

said information rewrite means temporarily returns the at least part of information to the information before being ciphered using the secret key.

17. (ORIGINAL) A processing apparatus according to claim 14, wherein

said processing apparatus comprises an information acquisition section for acquiring ciphered deciphering information to return said at least part of information to the information before being ciphered; and

said information rewrite means deciphers the ciphered deciphering information acquired by said information acquisition section, fetches deciphering information in plain text, and temporarily returns the at least part of information to the information before being ciphered using this deciphering information in plain text.

18. (ORIGINAL) A processing apparatus according to claim 1, wherein

said internal circuit holds a ciphering pattern adopted by said ciphering section;

the processing apparatus further comprises a tamper detection section detecting tamper; and

ciphering pattern destruction means for destroying the ciphering pattern held in said internal circuit in response to tamper detection made by said tamper detection section.

19. (PREVIOUSLY PRESENTED) A processing apparatus according to claim 11, wherein

said internal circuit holds a ciphering pattern adopted by said ciphering section;

the processing apparatus further comprises a tamper detection section detecting tamper; and

ciphering pattern destruction means for destroying the ciphering pattern held in said internal circuit in response to tamper detection made by said tamper detection section.

20. (CURRENTLY AMENDED) An integrated circuit constituted by mounting:

a CPU executing programs and is supplied with a first clock and executes the programs synchronously with the supplied first clock;

at least one internal device having a predetermined function, wherein at least one internal device is an internal memory, the internal memory storing a program for determining ciphering patterns;

a bus line extending internally of the integrated circuit and connecting said CPU to said internal device, the bus line comprising an externally extending portion extending externally of the integrated circuit and an address bus and a data bus, wherein at least one external device having a predetermined function is provided externally of integrated circuit and connected with the externally extending portion of the bus line, and the bus line transferring an address and data via the address bus and the data bus, respectively, wherein at least one external device is an external memory; and

a ciphering section interposed at an entrance to an external side of the integrated circuit, and ciphering the address and the data on the bus line by the ciphering patterns according to a plurality of regions divided from a space allotted to entirety of the at least one external device, to thereby prevent illicit access to the internal memory via the external memory, said ciphering section is supplied with a second clock and conducts ciphering synchronously with the supplied second clock and operates with the second clock at a higher speed than a speed of the first clock with which said CPU operates.

21. (ORIGINAL) An integrated circuit according to claim 20, wherein

the ciphering patterns adopted by the ciphering section include one ciphering pattern in which neither the address nor data is ciphered.

22. (ORIGINAL) An integrated circuit according to claim 20, wherein

in case where a plurality of external devices are provided externally of the externally extending portion of said bus line, said ciphering section performs ciphering by the ciphering patterns according to said plurality of external devices, respectively.

23. (ORIGINAL) An integrated circuit according to claim 20, wherein

said ciphering section outputs a dummy address and dummy data to the externally extending portion of said bus line at timing at which said external circuit is not accessed.

24. (CANCELLED)

25. (ORIGINAL) An integrated circuit according to claim 20, comprising:

ciphering pattern determination means for recognizing a constitution of said external circuit, and for determining a ciphering pattern of said ciphering section according to the constitution.

26. (ORIGINAL) An integrated circuit according to claim 20, wherein

said ciphering section ciphers the address and the data on said bus line by ciphering patterns according to the plurality of regions divided from the address space allotted to the entirety of said no less than one external device and according to application programs executed by said CPU.

27. (ORIGINAL) An integrated circuit according to claim 20, comprising:

ciphering pattern change means for changing a ciphering pattern whenever a predetermined initialization operation is performed, for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device.

28. (ORIGINAL) An integrated circuit according to claim 20, wherein

said ciphering section ciphers the data by adopting a ciphering pattern in which ciphered data is changed according to the address, for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device.

29. (CURRENTLY AMENDED) An integrated circuit comprising:

a CPU executing programs;

at least one internal device having a predetermined function, wherein at least one internal device is an internal memory~~, the internal memory storing a program for determining ciphering patterns~~; and

a bus line extending internally of the integrated circuit and connecting said CPU to said internal device, the bus line comprising an externally extending portion extending externally of the integrated circuit, and an address bus and a data bus, wherein an external circuit including at least one external memory as an external device storing information is provided externally of integrated circuit and connected with the externally extending portion of the bus line, and transferring an address and data via the address bus and the data bus, respectively; wherein

the integrated circuit includes information rewrite means for ciphering and rewriting at least part of the information stored in said external memory in a predetermined initialization operation, to thereby prevent illicit access to the internal memory via the external memory and said predetermined initialization operation is an initialization operation when the apparatus is first powered on.

30. (CANCELLED)

31. (ORIGINAL) An integrated circuit according to claim 29, wherein

said information rewrite means generates a random number, adopts a ciphering pattern using the generated random number and thereby performs ciphering.

32. (PREVIOUSLY PRESENTED) An integrated circuit according to claim 29, wherein

at least part of the information stored in said external memory has been already ciphered before said predetermined initialization operation is carried out; and

said information rewrite means temporarily returns the at least part of the information to information which is not ciphered, and rewrites the information by ciphering again the information by adopting a different ciphering pattern.

33. (PREVIOUSLY PRESENTED) An integrated circuit according to claim 32, wherein

deciphering information for returning said at least part of information to information before being ciphered is stored in the external memory; and

said information rewrite means temporarily returns said at least part of information to the information before being ciphered using the deciphering information.

34. (ORIGINAL) An integrated circuit according to claim 32, wherein

said at least part of information is ciphered by a public key, and a secret key is embedded in this processing apparatus; and

said information rewrite means temporarily returns the at least part of information to the information before being ciphered using the secret key.

35. (ORIGINAL) An integrated circuit according to claim 32, wherein

said processing apparatus comprises an information acquisition section for acquiring ciphered deciphering information to return the at least part of information to the information before being ciphered may be provided; and

said information rewrite means deciphers the ciphered deciphering information acquired by said information acquisition section, fetches deciphering information in plain text, and temporarily returns the at least part of information to the information before being ciphered using this deciphering information in plain text.

36. (CURRENTLY AMENDED) An apparatus comprising:

an internal circuit comprising:

a CPU to execute programs,

an internal device having a predetermined function, and

a bus line extending internally of the internal circuit and connecting the CPU to the internal device, the bus line comprising an externally extending portion extending externally of the internal circuit and an address bus and a data bus transferring an address and data, respectively; and

an external circuit comprising a external device having a predetermined function connected with the externally extending portion of the bus line,

wherein the internal circuit comprises an internal memory as an internal device~~, the internal memory storing a program for determining ciphering patterns~~, a predetermined initialization operation that is performed when the apparatus is first powered on and a means for ciphering the address and the data by the ciphering patterns according to regions divided from an address space allotted to the external device, and the external circuit includes an external memory as an external device wherein the ciphering patterns include at least one ciphering pattern in which neither the address nor the data is ciphered.